To the Claims:

Please amend the claims as follows.

Claim 1. (currently amended) A circuit for enhancing motion picture quality, comprising:

a first dual-port buffer, for receiving and temporarily storing a first frame ~~date~~ data, and first-in-first-out outputting said first frame data;

a second dual-port buffer, for receiving and temporarily storing a second frame ~~date~~data, and first-in-first-out outputting said second frame data; said first frame data being shown in a motion picture after said second frame data;

a frame memory, for storing a motion picture data;

a multiplexer unit, coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory, for selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said second frame data from said frame memory to said second dual-port buffer; and

a ~~signal-converter~~signal-converter, for ~~obtaining~~receiving said first frame data and said second frame data and comparing said first frame data and said second frame data to generate a compensation data [[to]]and output a third frame data ~~in response to said first frame data and said second frame data corresponding to said first frame data~~.

Claim 2. (currently amended) The circuit of claim 1, further comprising:

a first data latch, for receiving a fourth frame data and outputting said first frame data, the number of bits of said first frame data is larger than the number of bits of said fourth frame data;

a second data latch, for receiving ~~a fifth~~said second frame data and outputting

~~said seconda~~ fifth frame data, the number of bits of said second frame data is larger than the number of bits of said fifth frame data;

wherein said ~~signal converter~~signal-converter is for obtaining said compensation data to output said third frame data in response to said fourth frame data and said fifth frame data corresponding to said second frame data.

Claim 3. (currently amended) The circuit of claim 2, further comprising a nonlinear quantizer receiving a sixth frame data and quantizing said sixth frame data by using a nonlinear quantization method to output said fourth frame data, said ~~signal converter~~signal-converter receiving said sixth frame data and compensating said sixth frame data based on said compensation data to obtain said third frame data.

Claim 4. (currently amended) The circuit of claim 3, wherein said ~~signal converter~~signal-converter comprises:

a motion picture enhancing unit, for simultaneously receiving said fourth frame data and said fifth frame data and comparing said fourth frame data and said fifth frame data to generate said compensation data based on the difference between said fourth frame data and said fifth frame data; and

a data processing unit, for simultaneously receiving said sixth frame data and said compensation data corresponding to said sixth frame data, and compensating said sixth frame data based on said compensation data to obtain said third frame data.

Claim 5. (currently amended) The circuit of claim 2, wherein the number of bits of said first frame data are integral of the number of bits of said fourth frame data, and the number of bits of said second frame data ~~are~~is said integral of the number of bits of said fifth frame data.

Claim 6. (original) The circuit of claim 1, wherein said circuit is applied to a

liquid crystal display.

Claim 7. (currently amended) A circuit for enhancing motion picture quality, comprising:

a nonlinear quantizer receiving a first frame data and quantizing said first frame data by using a nonlinear quantization method to output a second frame data;

a frame memory module, coupled to said nonlinear quantizer, for receiving said second frame data and outputting a third frame data corresponding to said second frame data, said second frame data being shown in a motion picture after said third frame data; and

a ~~signal converter~~signal-converter, in response to said second frame data and said third frame data corresponding to said second frame data, for obtaining a compensation data to compensate said first frame data for outputting a fourth frame data.

Claim 8. (currently amended) The circuit of claim 7, wherein said frame memory module comprises:

a first dual-port buffer, for receiving and temporarily storing said second frame ~~date~~data, and first-in-first-out outputting said second frame data;

a second dual-port buffer, for receiving and temporarily storing said third frame ~~date~~data, and first-in-first-out outputting said third frame data;

a frame memory, for storing a motion picture data; and

a multiplexer unit, coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory; for selecting and transmitting one of said outputted said second frame data to said frame memory and said outputted said third frame data [[to]]from said frame memory to said second dual-port buffer.

Claim 9. (currently amended) The circuit of claim 8, wherein said ~~signal converter~~signal-converter comprises:

a motion picture enhancing unit, for simultaneously receiving said second frame data and said third frame data and comparing said second frame data and said ~~second~~ third frame data to generate said compensation data based on the difference between said second frame data and said third frame data; and

a data processing unit, for simultaneously receiving said first frame data and said compensation data corresponding to said first frame data, and compensating said first frame data based on said compensation data to obtain said fourth frame data.

Claim 10. (original) The circuit of claim 8, wherein said circuit is applied to a liquid crystal display.

Claim 11. (currently amended) A method for enhancing motion picture quality, comprising:

providing a first dual-port buffer, a second dual-port buffer, and a frame memory;

using said first dual-port buffer to receive and temporarily store a first frame ~~date~~data, and ~~first~~-in-first-out outputting said first frame data;

using said second dual-port buffer to receive and temporarily store a second frame ~~date~~data, and first-in-first-out outputting said second frame data; said first frame data being shown in a motion picture after said second frame data;

using said frame memory to store a motion picture data;

multiplexing said motion picture data in said frame memory thereby selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said second frame data from said frame memory to said second dual-port

buffer; and

obtaining a compensation data to output a third frame data in response to said

Claim 12. (currently amended) The method of claim 11, further comprising:

receiving a fourth frame data and outputting said first frame data, the number of bits of said first frame data is larger than the number of bits of said fourth frame data;

receiving ~~a fifth~~said second frame data and outputting ~~said seconda~~ fifth frame data, the number of bits of said second frame data is larger than the number of bits of said fifth frame data;

wherein said step of outputting said third frame data is performed by obtaining said compensation data in response to said fourth frame data and said fifth frame data corresponding to said second frame data.

Claim 13. (original) The method of claim 12, further comprising quantizing said sixth frame data by using a nonlinear quantization method to output said fourth frame data, wherein said step of outputting said third frame data further comprises:

simultaneously receiving said fourth frame data and said fifth frame data and comparing said fourth frame data and said fifth frame data to generate said compensation data based on the difference between said fourth frame data and said fifth frame data; and

simultaneously receiving said sixth frame data and said compensation data corresponding to said sixth frame data, and compensating said sixth frame data based on said compensation data to obtain said third frame data.

Claim 14. (currently amended) The method of claim 11, further comprising quantizing ~~saida~~ fourth frame data by using a nonlinear quantization method to output

buffer; and

obtaining a compensation data to output a third frame data in response to said first frame data and said second frame data corresponding to said first frame data.

Claim 12. (currently amended) The method of claim 11, further comprising:

receiving a fourth frame data and outputting said first frame data, the number of bits of said first frame data is larger than the number of bits of said fourth frame data;

receiving ~~a fifth~~said second frame data and outputting ~~said seconda~~ fifth frame data, the number of bits of said second frame data is larger than the number of bits of said fifth frame data;

wherein said step of outputting said third frame data is performed by obtaining said compensation data in response to said fourth frame data and said fifth frame data corresponding to said second frame data.

Claim 13. (original) The method of claim 12, further comprising quantizing said sixth frame data by using a nonlinear quantization method to output said fourth frame data, wherein said step of outputting said third frame data further comprises:

simultaneously receiving said fourth frame data and said fifth frame data and comparing said fourth frame data and said fifth frame data to generate said compensation data based on the difference between said fourth frame data and said fifth frame data; and

simultaneously receiving said sixth frame data and said compensation data corresponding to said sixth frame data, and compensating said sixth frame data based on said compensation data to obtain said third frame data.

Claim 14. (currently amended) The method of claim 11, further comprising quantizing ~~saida~~ fourth frame data by using a nonlinear quantization method to output

comprises:

simultaneously receiving said first frame data and said second frame data and comparing said first frame data and said second frame data to generate said compensation data based on the difference between said first frame data and said second frame data; and

simultaneously receiving said fourth frame data and said compensation data corresponding to said fourth frame data, and compensating said fourth frame data based on said compensation data to obtain said third frame data.

Claim 15. (currently amended) A circuit for enhancing motion picture quality, comprising:

a first dual-port buffer receiving and temporarily storing a first frame [[date]]data, and first-in-first-out outputting said first frame data;

a second dual-port buffer, for receiving and temporarily storing a second frame [[date]]data, and first-in-first-out outputting said second frame data; said first frame data being shown in a motion picture after said second frame data;

a frame memory, for storing a motion picture data;

a multiplexer unit, coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory, for selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said second frame data from said frame memory to said second dual-port buffer;

a ~~signal converter, in response to said first frame data, a third frame data and said second frame data corresponding to said third frame data, for obtaining a compensation data~~signal-converter, for receiving said first frame data, said second

said first frame data, wherein said step of outputting said third frame data further comprises:

simultaneously receiving said first frame data and said second frame data and comparing said first frame data and said second frame data to generate said compensation data based on the difference between said first frame data and said second frame data; and

simultaneously receiving said fourth frame data and said compensation data corresponding to said fourth frame data, and compensating said fourth frame data based on said compensation data to obtain said third frame data.

Claim 15. (currently amended) A circuit for enhancing motion picture quality, comprising:

a first dual-port buffer receiving and temporarily storing a first frame [[date]]data, and first-in-first-out outputting said first frame data;

a second dual-port buffer, for receiving and temporarily storing a second frame [[date]]data, and first-in-first-out outputting said second frame data; said first frame data being shown in a motion picture after said second frame data;

a frame memory, for storing a motion picture data;

a multiplexer unit, coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory, for selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said second frame data from said frame memory to said second dual-port buffer;

a ~~signal converter, in response to said first frame data, a third frame data and said second frame data corresponding to said third frame data, for obtaining a compensation data~~signal-converter, for receiving said first frame data, said second

frame data and a third frame data to generate a compensation data and to output a fourth frame data and a fifth frame data;

a first data flow switcher, for receiving a sixth frame data and a seventh frame data and transforming said sixth frame data and said seventh frame data ~~into one of said first frame data and said third frame data respectively and said third frame data and said first frame data respectively~~to output said first frame data and said third frame data, said first data flow switcher outputs one of said first frame data and said third frame data; and

a second data flow switcher, for receiving said fourth frame data and said fifth frame data and transforming said fourth frame data and said fifth frame data ~~into one of said eighth frame data and said ninth frame data respectively and said eighth frame data and said ninth frame data respectively~~to output an eighth frame data and a ninth frame data, said second data flow switcher outputs one of said eighth frame data and said ninth frame data.

Claim 16. (currently amended) The circuit of claim 15, further comprising:

a first data latch, coupled to and between said first data flow switcher and said first dual-port buffer, said first data flow switcher is changed for receiving said sixth frame data and said seventh frame data, and transforming said sixth frame data and said seventh frame data ~~into one of a tenth frame data and said third frame data respectively and said third frame data and said tenth frame data respectively~~to output a tenth frame data and the third frame data, said first data flow switcher outputs one of said third frame data and said tenth frame data, said first data latch, for receiving said tenth frame data and outputting said first frame data, the number of bits of said first frame data is larger than the number of bits of said tenth frame data;

a second data latch, coupled to and between said first dual-port buffer and said ~~signal-converter~~signal-converter, for receiving said second frame data and outputting an eleventh frame data, the number of bits of said second frame data is larger than the number of bits of said eleventh frame data;

wherein said ~~signal-converter~~signal-converter, in response to said tenth frame data, said third frame data and said eleventh frame data corresponding to said third frame data, obtains said compensation data to output said fourth frame data and said fifth frame data.

Claim 17. (currently amended) The circuit of claim 16, further comprising:

a first nonlinear quantizer, coupled to and between said first data flow switcher and said first data latch, said first data flow switcher is changed for receiving said sixth frame data and said seventh frame data, and transforming said sixth frame data and said seventh frame data ~~into one of a twelfth frame data and said third frame data respectively and said third frame data and said twelfth frame data respectively~~to output a twelfth frame data and the third frame data, said first data flow switcher outputs one of said third frame data and said twelfth frame data, said first nonlinear quantizer receiving said twelfth frame data and quantizing said twelfth frame data by using a nonlinear quantization method to output said tenth frame data; and

a second nonlinear quantizer, coupled to and between said first data flow switcher and said ~~signal-converter~~signal-converter, for receiving said third frame data and quantizing said third frame data by using a nonlinear quantization method to output said thirteenth frame data;

wherein said ~~signal-converter~~signal-converter, in response to said twelfth frame data, said third frame data, and said thirteenth frame data corresponding to said

eleventh frame data, obtains said compensation data to output said fourth frame data and said fifth frame data.

Claim 18. (currently amended) The circuit of claim 17, wherein said ~~signal converter~~signal-converter comprises:

a motion picture enhancing unit, for simultaneously receiving said thirteenth frame data and said eleventh frame data and comparing said thirteenth frame data and said eleventh frame data to generate said compensation data based on the difference between said thirteenth frame data and said eleventh frame data;

a first data processing unit, for simultaneously receiving said twelfth frame data and said compensation data corresponding to said twelfth frame data, and compensating said twelfth frame data based on said compensation data to obtain said fourth frame data; and

a second data processing unit, for simultaneously receiving said third frame data and said compensation data corresponding to said third frame data, and compensating said third frame data based on said compensation data to obtain said fifth frame data.

Claim 19. (original) The circuit of claim 16, wherein the number of bits of said first frame data are integral of the number of bits of said tenth frame data, and the number of bits of said second frame data are said integral of the number of bits of said eleventh frame data.

Claim 20. (original) The circuit of claim 15, wherein said circuit is applied to a liquid crystal display.

Claim 21. (currently amended) A circuit for enhancing motion picture quality, comprising:

a first nonlinear quantizer, for receiving a first frame data and quantizing said

first frame data by using a nonlinear quantization method to output a second frame data;

a second nonlinear quantizer, for receiving a third frame data and quantizing said third frame data by using a nonlinear quantization method to output a fourth frame data;

a frame memory module, coupled to said first nonlinear quantizer, receiving said second frame data and outputting a fifth frame data corresponding to said second frame data, said second frame data being shown in a motion picture after said fifth frame data;

a ~~signal converter, in response to said first frame data, said third frame data, said fourth frame data and said fifth frame data corresponding to said fourth frame data, for obtaining a compensation data~~signal converter, for receiving said first frame data, said third frame data, said fourth frame data and said fifth frame data to generate a compensation data and to output a sixth frame data and a seventh frame data;

a first data flow switcher, for receiving an eighth frame data and a ninth frame data and transforming said eight frame data and said ninth frame data ~~into one of said first frame data and said third frame data respectively and said third frame data and said first frame data respectively~~to output the first frame data and the third frame data, said first data flow switcher outputs one of said first frame data and said third frame data; and

a second data flow switcher, for receiving said sixth frame data and said seventh frame data and transforming said sixth frame data and said seventh frame data ~~into one of said tenth frame data and said eleventh frame data respectively and said tenth frame data and said eleventh frame data respectively~~to output a tenth frame data and a eleventh frame data, said second data flow switcher outputs one of said tenth frame data and said eleventh frame data.

Claim 22. (currently amended) The circuit of claim 21, wherein said frame memory module comprises:

a first dual-port buffer, for receiving and temporarily storing said second frame [[date]]data, and first-in-first-out outputting said second frame data;

a second dual-port buffer, for receiving and temporarily storing said fifth frame [[date]]data, and first-in-first-out outputting said fifth frame data;

a frame memory storing a motion picture data; and

a multiplexer unit, coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory; for selecting and transmitting one of said outputted said second frame data to said frame memory and said outputted said fifth frame data from said frame memory to said second dual-port buffer.

Claim 23. (currently amended) The circuit of claim 22, wherein said ~~signal converter~~signal-converter comprises:

a motion picture enhancing unit, for simultaneously receiving said fourth frame data and said fifth frame data and comparing said fourth frame data and said fifth frame data to generate said compensation data based on the difference between said fourth frame data and said fifth frame data;

a first data processing unit, for simultaneously receiving said first frame data and said compensation data corresponding to said first frame data, and compensating said first frame data based on said compensation data to obtain said sixth frame data.; and

a second data processing unit, for simultaneously receiving said third frame data and said compensation data corresponding to said third frame data, and compensating said third frame data based on said compensation data to obtain said seventh frame data.

Claim 24. (original) The circuit of claim 21, wherein said circuit is applied to a

liquid crystal display.

Claim 25. (currently amended) A method for enhancing motion picture quality, comprising:

providing a first dual-port buffer, a second dual-port buffer, and a frame memory;

using said first dual-port buffer to receive and temporarily store a first frame [[date]]data, and first-in-first-out outputting said first frame data;

using said second dual-port buffer to receive and temporarily store a second frame [[date]]data, and first-in-first-out outputting said second frame data; said first frame data being shown in a motion picture after said second frame data;

using said frame memory to store a motion picture data;

multiplexing said motion picture data in said frame memory thereby selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said second frame data from said frame memory to said second dual-port buffer; and

obtaining a compensation data to output a fourth frame data and a fifth frame data, in response to said first frame data, a third frame data, and said second frame data corresponding to said third frame data;

transforming a sixth frame data and a seventh frame data into one of said first frame data and said third frame data respectively and said third frame data and said first frame data respectively, in response to a time sequence; and

transforming said fourth frame data and said fifth frame data into one of an eighth frame data and a ninth frame data respectively and said ninth frame data and said eighth frame data respectively, in response to said time sequence.